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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/650,403
Filing Date: August 28, 2003
Appellant(s): CHEUNG, HUGO

Alan K. Stewart (Reg. No. 35,373)
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed December 21, 2007 appealing from the Office action mailed June 23, 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct. Note that claim 18 is withdrawn from consideration on appeal.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct. Note that claim 18 is withdrawn from consideration on appeal. Claim 18 is therefore not listed in the Claims Appendix.

(8) Evidence Relied Upon

5,278,956	Thomsen et al.	01-1994
US 2002/0078317 A1	Yasoshima	04-2002

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

1. Claim 18 is rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for "receiving and storing the new data in a receive shift register in a location of said buffer designated by **a shift pointer**" [page 12, ll. 12-20; FIG. 4], **does not** reasonably provide enablement for "receiving and storing the new data in a receive shift register in a location of said buffer designated by **a read pointer**". The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to use the invention commensurate in scope with these claims.

Page 12, ll. 14-16 discloses "The RdPtr pointer comprises the location of the FIFO buffer 400 that the CPU will read from during data transmission, and is configured to increment after the CPU reads from the SPI data register" while page 16, ll. 7-10

discloses "a new byte of data can be suitably received and stored in the receive shift register 304, i.e., stored in the location of FIFO buffer 400 designated by the RdPtr pointer". It appears that the disclosure on page 16, ll. 7-10 contradicts the disclosure on page 12, ll. 14-16, FIG. 4, and the context of the invention. Furthermore, the disclosure only provides support for the read pointer being the RdPtr pointer, and does not provide support for read pointer to mean the ShfPtr pointer [FIG. 4].

2. Claims 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thomsen et al. (US 5,278,956) in view of Yasoshima (US 2002/0078317).

3. As per claims 15, Thomsen discloses an apparatus - hence a high performance buffering technique for use with a serial peripheral interface [FIG. 4; col. 6, ll. 3-19] to facilitate high data rates, said buffering technique comprising the steps of:

initializing a transmitter FIFO [18, FIG. 4] by writing data to a data register [writing data to location designated by write pointer of transmitter FIFO; col. 2, l. 66-col. 3, l. 23];

performing a transmit buffering sequence to prepare for the transmitting of the data [incrementing a write pointer of the transmitter FIFO and incrementing a counter representing the number of bytes in the transmitter FIFO [col. 2, l. 66-col. 3, l. 23]];

performing a transmit and receive shifting sequence to facilitate transmitting of the data and receiving of new data at substantially the same time [reading data from a location in the transmitter FIFO designated by a read pointer of the transmitter FIFO; writing the data to a transmit shift register [20, FIG. 4]; shifting of the transmit shift register [to communication station 17, FIG. 4]; and receiving and storing new data in a receive shift register [16, FIG. 4] in a location of a receiver FIFO [12, FIG. 4] designated

by a write pointer of the receiver FIFO [FIG. 4; col. 2, l. 66-col. 3, l. 23; col. 6, ll. 3-19] - the architecture of FIG. 4 with transmitter and receiver shift registers and transmitter and receiver FIFOs allows full duplex communication, hence facilitates transmitting of data from transmitter FIFO and receiving of new data by the receiver FIFO at substantially the same time]; and

performing a receive buffering sequence to prepare for the receipt of additional new data [incrementing a write pointer of the receiver FIFO to identify a new location for receiving data; and incrementing a counter to indicate that new data has been received [col. 2, l. 66-col. 3, l. 23]].

Thomsen, therefore, discloses the invention except for the transceiver FIFO and the receiver FIFO being arranged within a single buffer.

Yasoshima discloses arranging multiple FIFOs within a single buffer to accommodate applications processing distinct data segments and maximize the utilization of memory [[0006], ll. 1-4].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to arrange the transceiver FIFO and the receiver FIFO within a single buffer, as is taught by Yasoshima, because such arrangement would accommodate applications processing distinct data segments (as data transmitted by the CPU and data read by the CPU represent distinct data segments) and maximize the utilization of memory.

4. As per claims 16-17, Thomsen discloses writing the data into a location of said buffer as designated by a write pointer [col. 2, l. 66-col. 3, l. 23]; and incrementing a

write pointer to prevent a next byte to be transmitted from overwriting a previous written byte; and incrementing a write shift counter to facilitate tracking of a number of bytes available for transmission [col. 2, l. 66-col. 3, l. 23].

5. As per claims 18-19, Thomsen discloses reading the data from a location in the buffer designated by a read pointer of transmitter FIFO (i.e. a shift pointer - as explained below); writing the data to a transmit shift register; shifting of the transmit shift register; and receiving and storing the new data in a receive shift register in a location of said buffer designated by a write pointer of the receiver FIFO (i.e. a read pointer of the transmitter FIFO or the shift pointer - as explained below); incrementing a write pointer of receiver FIFO (i.e. a shift pointer - as explained below) to identify a new location in the buffer for receiving data; and incrementing a counter to indicate that the new data has been received [col. 2, l. 66-col. 3, l. 23]. Yasoshima discloses the read pointer of the transmitter FIFO functioning as a boundary for the receiver FIFO [FIG. 2(b); [0009]], hence a shift pointer (as the read pointer of the transmitter FIFO and the write pointer of the receiver FIFO will be at the same location after shifting of the shift registers).

6. As per claim 20, the combination of Thomsen and Yasoshima does not teach interrupting a CPU if the data is ready for transmitting and said buffer is approximately full, and interrupting the CPU if said buffer is ready to receive data and said buffer is approximately empty. Since it was known in the art the time the invention was made to interrupt a CPU when data is ready for transmitting and the buffer is approximately full to prevent buffer overflow, and to interrupt the CPU when the buffer is ready to receive data and the buffer is approximately empty to prevent buffer underflow, it would have

been obvious to one of ordinary skill in the art at the time the invention was made to incorporate such interruptions in order to prevent buffer overflow or buffer underflow.

(10) Response to Argument

A. Appellant argues that claim 15 includes "…initializing a single buffer to act as transmitter and receiver by writing data to a data register;…performing a transmit and receive shifting sequence to facilitate transmitting of the data and receiving of new data at substantially the same time…" and that the references of record does not show, teach, or suggest the limitations of claim 15.

Appellant's argument with respect to the references not suggesting "initializing a single buffer to act as transmitter and receiver by writing data to a data register" is not persuasive because:

Thomsen (USP 5,278,956) was relied upon to teach initializing a transmitter FIFO buffer **[FIFO 18, FIG. 4]** by writing data to a data register of the transmitter FIFO buffer **[writing data to a location designated by write pointer (write address counter 102 - FIG. 1) of the transmitter FIFO buffer; col. 2, line 66-col. 3, line 23]**.

Thomsen was also relied upon to teach a receiver FIFO buffer **[12, FIG. 4]**. Note that the receiver FIFO buffer [12, FIG. 4] is also initialized by writing data to a data register of the receiver FIFO buffer **[writing data to a location designated by write pointer (write address counter 102 - FIG. 1) of the receiver FIFO buffer; col. 2, line 66-col. 3, line 23]**.

Yasoshima (US 2002/0078317 A1) was relied upon to teach implementing

multiple FIFOs as a single buffer in order to accommodate applications processing distinct data segments and maximize the utilization of memory **[[0006], ll. 1-10]**.

Since the transmitter FIFO buffer of Thomsen is used for processing data to be transmitted to communication station 17 [FIG. 4], and the receiver FIFO buffer of Thomsen is used for processing data to be received from communication station 17 [FIG. 4], the data segments in the transmitter FIFO buffer of Thomsen are distinct from the data segments in the receiver FIFO buffer of Thomsen. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the transmitter FIFO buffer of Thomsen and the receiver FIFO buffer of Thomsen (multiple FIFOs) as a single buffer to accommodate the distinct data segments and to maximize the utilization of memory in the single buffer (as is suggested by Yasoshima).

The combination of Yasoshima with Thomsen would therefore suggest initializing a single buffer to act as transmitter and receiver by writing data to a data register.

Appellant's argument with respect to the references not suggesting "performing a transmit and receive shifting sequence to facilitate transmitting of the data and receiving of new data at substantially the same time" is not persuasive because:

Thomsen teaches performing a transmit and receive shifting sequence to facilitate transmitting of the data **[reading data from a location in the transmitter FIFO buffer designated by a read pointer (read address counter 100 - FIG. 1) of the transmitter FIFO buffer; writing the data to a transmitter shift register [21, FIG. 4]; shifting of the data in the transmitter shift register (to communication station**

17, FIG. 4)] and receiving of new data **[receiving new data (from communication station 17, FIG. 4) in receiver shift register [19, FIG. 4] and storing new data from receiver shift register in a location of a receiver FIFO buffer [12, FIG. 4] designated by a write pointer of the receiver FIFO buffer [FIG. 4; col. 2, l. 66-col. 3, l. 23; col. 6, ll. 3-19]** at substantially the same time **[the architecture of FIG. 4 with transmitter shift register, receiver shift register, transmitter FIFO buffer and receiver FIFO buffer allows data to be transmitted and new data to be received at substantially the same time because data is transmitted to the transmitter shift register independently of new data being received at the receiver shift register - hence facilitating transmitting of data and receiving of new data at substantially the same time]**.

Note that transmit shift register [20, FIG. 4] in the rejection is a typographical error, and should instead be transmit shift register [21, FIG. 4]. Note that receive shift register [16, FIG. 4] in the rejection is also a typographical error, and should instead be receive shift register [19, FIG. 4].

B. Appellant further argues that Yasoshima (US 2002/0078317 A1) does not disclose a single buffer to facilitate transmitting and receiving at substantially the same time.

Appellant's argument is not persuasive because "a single buffer to facilitate transmitting and receiving at substantially the same time" is not recited in the rejected claims. The claims merely require "…initializing a single buffer to act as transmitter and receiver by writing data to a data register;…performing a transmit and receive shifting

sequence to facilitate transmitting of the data and receiving of new data at substantially the same time…". Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Appellant's argument is also not persuasive because Yasoshima **alone** was not relied upon to teach a single buffer and facilitating transmitting and receiving at substantially the same time. Yasoshima was relied upon to teach implementing the transmitter FIFO buffer and the receiver FIFO buffer of Thomsen as a single buffer (see the examiner's response to appellant's argument in section A. above). Thomsen (USP 5,278,956) was relied upon to teach facilitating transmitting of the data and receiving of new data at substantially the same time (see the examiner's response to appellant's argument in section A. above). One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Appellant's argument is further not persuasive because "substantially" is a relative term that is not defined by the claims, and because the specification does not specifically disclose "at substantially the same time" **having the same meaning as** "at the same time". The claims therefore do not require for facilitating transmitting and receiving at the same time.

C. Applicant further argues that the references do not teach how the device of Yasoshima (US 2002/0078317 A1) can be combined with Thomsen (USP 5,278,956)

to obtain a single buffer for performing a transmit and receive shifting sequence to facilitate transmitting of the data and receiving of new data.

Appellant's argument is not persuasive because "a single buffer for performing a transmit and receive shifting sequence to facilitate transmitting of the data and receiving of new data" is not recited in the rejected claims. The claims merely require "…initializing a single buffer to act as transmitter and receiver by writing data to a data register;…performing a transmit and receive shifting sequence to facilitate transmitting of the data and receiving of new data at substantially the same time…". Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Appellant's argument is also not persuasive because Yasoshima was relied upon to teach implementing the transmitter FIFO buffer and the receiver FIFO buffer of Thomsen as a single buffer (see the examiner's response to appellant's argument in section A. above); and because Thomsen was relied upon to teach performing a transmit and receive shifting sequence to facilitate transmitting of the data and receiving of new data (see the examiner's response to appellant's argument in section A. above).

D. Note further that appellant indicates that claim 18 is withdrawn from consideration on appeal (see STATUS OF THE CLAIMS section). **The rejection of claim 18 is therefore considered acquiesced by appellant** - per MPEP 1205.02 [R-3]

> In accordance with the above, the brief must be directed to the claims and to the record of the case as they appeared at the time of the appeal, but it may, of course, withdraw from consideration on appeal any claims or issues as desired by appellant. Even if the appeal brief withdraws from consideration any claims or issues (i.e., appellant acquiesces to any rejection),

the examiner must continue to make the rejection in the examiner's answer, unless an amendment obviating the rejection has been entered.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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March 5, 2008